REMARKS

Claims 1-23 are pending in this application. Claims 1-5, 20, 22, and 23 are independent.

Information Disclosure Statement

The Information Disclosure Statement filed August 30, 2000 has not been acknowledged by the Examiner as to consideration of the reference cited therein. **Therefore, the Examiner is respectfully requested to provide Applicant with an initialed PTO-1449 Form, indicating consideration of the Information Disclosure Statement submitted August 30, 2000.**

Drawings

Figures 18 and 19 have been objected to as not being designated "Prior Art." Accordingly, The drawings in figures 18 and 19 have been corrected to show the label as required. Applicants respectfully request that the objection be withdrawn.

Abstract

The Abstract of the Disclosure has been objected to because it exceeds 150 words in length. Accordingly, Applicants have re-written the Abstract to be within 150 words. Applicants respectfully request that the objection be withdrawn.

Claim Rejection – 35 USC 112, second paragraph

Claims 1-5, 20, 22, and 23 have been rejected under 35 U.S.C. 112, second paragraph. Claims 1-5, 20, 22, and 23 have been amended in order to conform with current U.S. practice as required. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 USC 103

Claims 1-5, 20, 22, and 23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (U.S. Patent 6,300,823, "Zhou") in view of Hayashi (U.S. Patent 5,392,040). Applicants respectfully traverse this rejection.

Claim 1 is directed to a filter circuit comprising a plurality of unit circuits including a first stage unit circuit, at least one second stage unit circuit, and a final stage unit circuit mutually connected in series. Each of the unit circuits comprises a computing means. The computing means in each of the first stage unit circuit and the at least one second stage unit circuit successively transmitting to a unit circuit of a following stage unit circuit a computing result of a) an analog input signal sampled at a sampling timing and b) a coefficient predetermined for each computing means. The computing result being computed by adding a value of a residual, from a previous stage unit circuit and a computing result based on the analog input signal and a coefficient for the computing means to obtain an added value (e.g., output of K12), low-bit quantizing the added value to obtain a quantization result (e.g., output of Q2), subtracting a D/A converted value of the quantization result

from the added value to obtain a residual value (e.g., output of K32), and successively transmitting said quantization result as the computing result and the residual value to a following circuit.

The Office Action points to a variety of items as teaching the claimed stages of unit circuits. In particular, the Office Action states that Zhou's sampling and holding means 10 teaches the claimed plurality of unit circuits, coefficient registers 20 and multiplication circuits 30 in Zhou correspond to the claimed previous stage, sampling and holding circuits 30 in Zhou correspond to the claimed present stage, and the adder 70 corresponds to the claimed final stage.

However, the claimed computing means in each of the unit circuits successively transmits to a unit circuit of a following stage a computing result of an analog input signal and a coefficient. In other words, in the present invention, unit circuits constitute each stage that is connected in series.

On the other hand, in Zhou even though the sampling and holding means appear to be connected in series, they each provide values to the multiplication circuit in parallel, then to adder 40 in parallel. The adder 40 sums up the computing results. However, no quantization is then performed on the computing results, as in the claimed invention.

Thus, Applicants submit that Zhou fails to teach or suggest unit circuits connected in series and each of the unit circuits comprising computing means in the first stage unit circuit and at least one second stage unit circuit successively transmitting to a unit circuit of a following stage unit circuit a

computing result of an analog input signal and a coefficient predetermined for each computing means. Such a limitation is found in independent claims 1-5.

Independent claims 20, 22, and 23 are directed to a filter circuit having a plurality of correlation computing unit circuits for performing a predetermined computing on an analog input signal. The correlation computing circuits are connected in series. Applicants submit that Zhou's sampling and holding circuits do not teach the claimed correlation computing circuits.

Hayashi is relied on for teaching a low-bit quantization and a D/A converter. Hayashi discloses a quantization circuit that is part of a D/A converter and that converts a digital input signal into a digital input signal having a fewer number of bits.

In the present invention, on the other hand, the low-bit quantization is performed on an analog input signal. In claim 1, for example, the computing result of the computing means of each unit circuit is computed by adding a value of a residual (e.g., output of adder K31, Fig. 1), from a previous stage unit circuit and a computing result based on the analog input signal (e.g., Analog Input Signal Sm), and a coefficient for the computing means to obtain an added value (e.g., output of adder K12), then low-bit quantizing (e.g., Quantization circuit Q1) the added value (i.e., an analog signal). The other claims are directed to comparable structure.

Thus, Applicants submit that Hayashi fails to make up for the deficiency in Zhou. Therefore, Applicants submit that the rejection fails to establish *prima*

facie obviousness. Applicants respectfully request that the rejection be withdrawn.

CONCLUSION

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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Attachments: Abstract of the Disclosure
Replacement Sheets (Figs. 18 and 19)
PTO-1449 Form

Abstract of the Disclosure

In a filter circuit of the present invention, a partial quantization value is computed by a quantization circuit according to a spread code and others in a unit at an arbitrary stage, where an integrating value is increased. The partial quantization value is successively added by an adder formed by a counter and is transmitted to a unit of the following stage. In an adder of the following stage, an analog residual is computed by subtracting an analog converted value of the partial quantization value, that is obtained by a D/A converter, from the integrating value so as to suppress an increase in the analog cumulative value. With this arrangement, the cumulative value is increased according to an increase in the number of taps, so that an analog adder can reduce power consumption, which is caused by expansion of a dynamic range at the following stage.